東楠科技股份有限公司
Tungnan Technology Co., Ltd.

LED DRIVER

M1357

4-CHANNEL LED DIMMER DRIVER

GENERAL DESCRIPTION

The M1357 is a monolithic, 4-channel NMOS PWM LED drivers Controller can also be directly programmed through an Serial Bus Micro-Processor Interface for applications where user defined LED pattern, color, and intensity programmability is a priority. Optimized for dimming LEDs in 256 discrete steps for Red/Green/Blue (RGB) color mixing and back light applications.

The M1357 includes an internal oscillator , four individual PWM color LED drivers and The open drain outputs directly drive the LEDs with constant sink current of 15mA per bit.

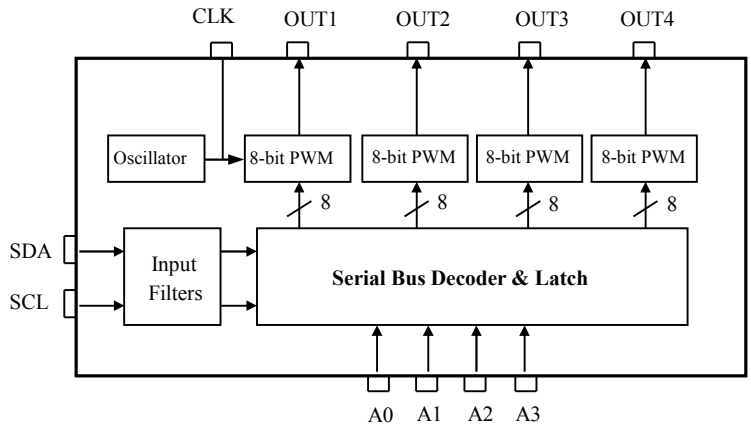
FEATURES

- 4 open drain outputs directly drive LEDs
- Constant sink current of 15mA per bit
- 256 brightness steps
- A0~A3 is External address selection.
- Internal oscillator requires no external components
- Controlled by Serial Bus Micro-Processor Interface
- Internal power-on reset
- Noise filter on SCL/SDA inputs

APPLICATIONS

- True color LED display driver

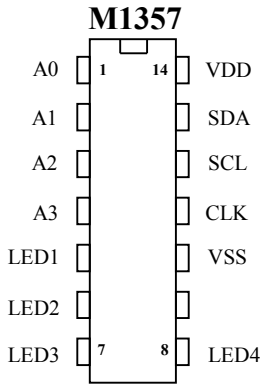
BLOCK DIAGRAM



4-CHANNEL LED DIMMER DRIVER

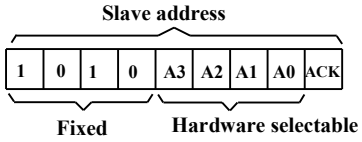
PIN DESCRIPTION

Pin No	Pin Name	Description
1~4	A0~A3	Address input
5~8	LED1~LED4	LED driver1~4
10	VSS	Negative power supply
11	CLK	system clock output (~ 225KHz)
12	SCL	Serial clock line
13	SDA	Serial data line
14	VDD	Positive power supply.

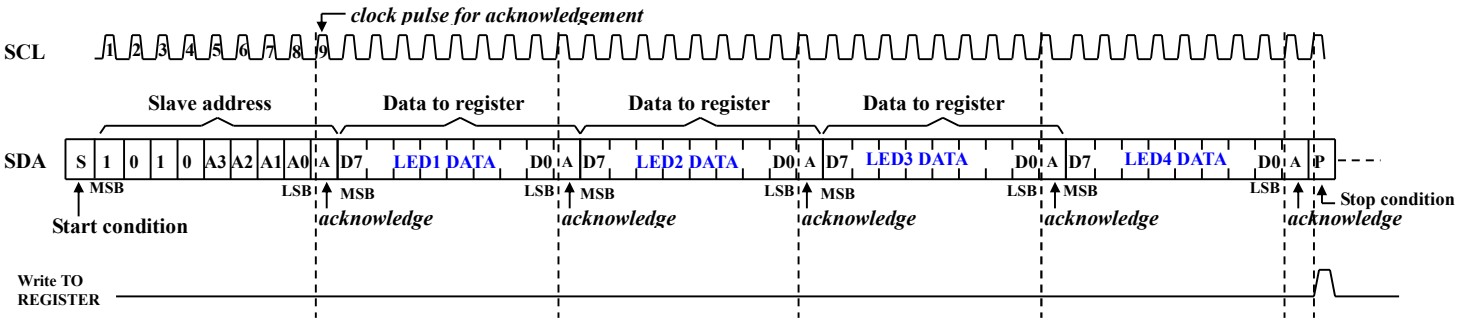


DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the M1357 is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.



WRITE to Register



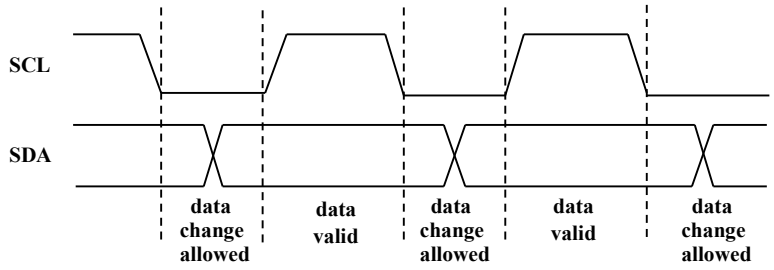
Note:

1. D7-D0：Sets Brightness for LED1~ LED4 DATA (Data to register). 11111111= Full scale
2. Acknowledge：

   The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a LOW level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

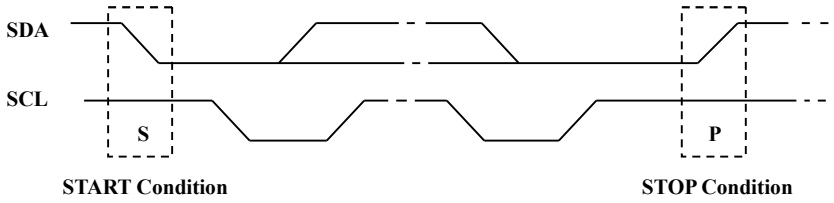
DATA VALIDITY

The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.



START and STOP conditions

START and STOP conditions classify the beginning and the end of the Serial Bus session. A START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The Serial Bus master always generates START and STOP conditions. The Serial Bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the Serial Bus master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



TRANSFERING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse.

4-CHANNEL LED DIMMER DRIVER

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
VDD	Supply voltage		-0.5	6.0	V
ISS	Supply current		—	100	mA
Ptot	Total power dissipation		—	400	mW
Tstg	Storage temperature range		-65	+150	°C
Tamb	Operating ambient temperature		-20	+85	°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

DC CHARACTERISTICS

SYMBO	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
VDD	Supply voltage		4.5	5	5.5	V
IDD	Supply current	Operating mode；VDD = 5.5V；No load；VI = VDD or VSS；f_{SCL}= 100KHz	—	700	1000	μA
Input SCL,SDA						
VIL	LOW-level input voltage		-0.5	—	0.2 VDD	V
VIH	HIGH-level input voltage		0.6 VDD	—	5.5	V
IL	Leakage current	VI = VDD = VSS	-1	—	+1	μA
CI	Input capacitance	VI = VSS	—	5	10	pF

NOTE：Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

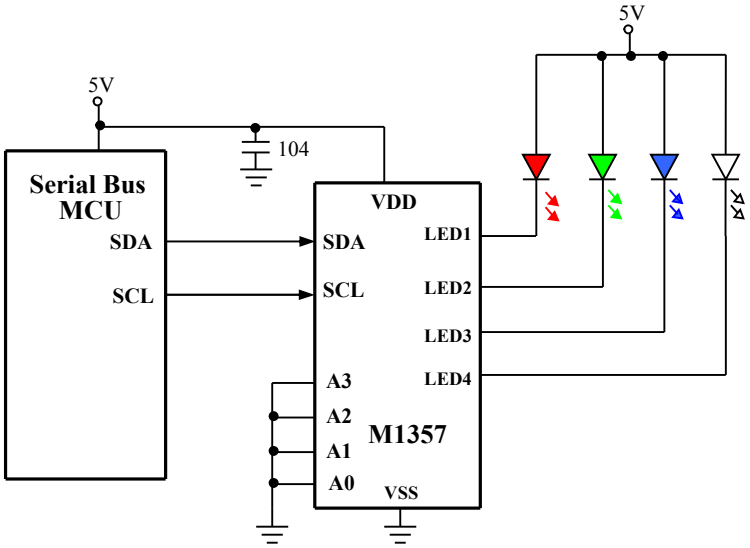
AC SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
f_{SCL}	Operating frequency	0	400	KHz
f_{BUF}	Bus free time between STOP and START conditions	1.3	—	μs
$t_{HD；STA}$	Hold time after (repeated) START condition	0.6	—	μs
$t_{SU；STA}$	Repeated START condition setup time	0.6	—	μs
$t_{SU；STO}$	Setup time for STOP condition	0.6	—	μs
$t_{HD；DAT}$	Data in hold time	0	—	ns
$t_{SU；DAT}$	Data setup time	0.6	—	μs
t_{LOW}	Clock LOW period	1.3	—	μs
t_{HIGH}	Clock HIGH period	0.6	—	μs
t_F	Clock/Data fall time	20 + 0.1 Cb1	300	ns
t_R	Clock/Data rise time	20 + 0.1 Cb1	300	ns

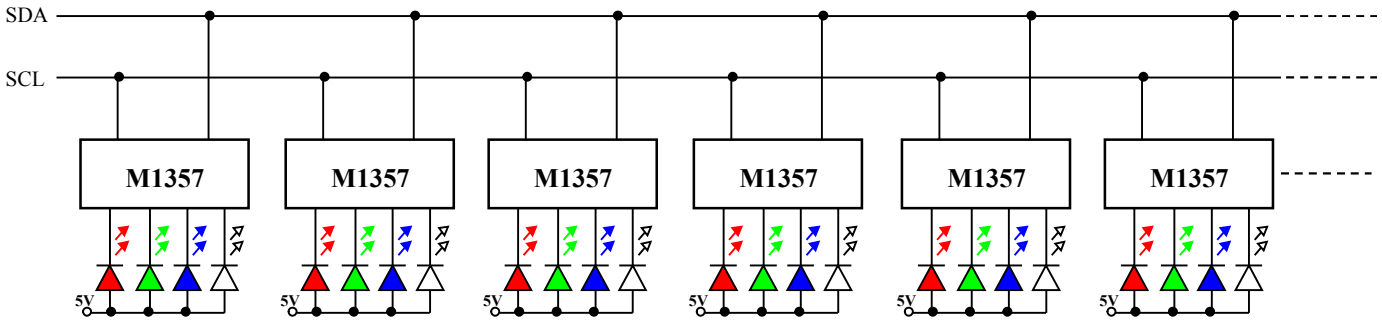
1. Cb = total capacitance of one bus line in pF.

4-CHANNEL LED DIMMER DRIVER

TYPICAL APPLICATION



LED SYSTEM CONFIGURATION



* All specs and applications shown above subject to change without prior notice.
(以上電路及規格僅供參考,本公司得逕行修正)